Bipolar Junction Transistors - Week 14 (April 21st and April 23rd 2020)

LAB 14: Simulating circuits using bipolar junction transistors: Common Emitter, Emitter Follower, Dual stage and Darlington Pair

GOALS

In this lab we will simulate and study the performance of the common emitter and emitter follower circuits, which use bipolar junction transistors (BJTs). In addition, we introduce the widely used Darlington Pair configuration.

PRE-LAB ACTIVITIES

A. You should review the Lab 7 manual on the theory of BJT operation and the basics of the common emitter and emitter follower circuits. Review your pre-lab calculations as well.

B. At this point, you should be getting *proficient* with using LTSpice. Please review Lab 11 and 12 manuals and supplemental materials, if needed. We will introduce a new technique with this lab: using net labels to form connections without wires.

LAB ACTIVITIES

Step 1: Build a generic signal voltage source with output impedance and a simple resistive load.

The ideal voltage source of LTSpice has zero output impedance but real signal sources do. Ideally they are small, but not always. We will use a Thevenin equivalent model for the signal source, which is an ideal voltage source in series with a resistance Ros, the output impedance of the signal generator. We'll attach it to a load resistor just to introduce the promised LTSpice technique.

(a) Open a new asc file and create the signal source shown in Figure 1, from a voltage source and resistor. Right click on the right end of the resistor; a menu will come up, choose "Label Net" (the same thing you do to create grounds). Instead of making it a ground, type in the new label Vin. Give the resistor a value of 1kΩ and set the voltage supply to give you a 15kHz sine wave of amplitude 100 mV with no DC offset. This is your signal generator, which at the moment has a large output impedance of 1kΩ.

(b) Now somewhere to the right (also as shown in Fig. 1), create a load resistance RLoad, also of value 1kΩ, which is connected to ground. Label the other end of the load resistor Vout.

(c) Now you can connect your signal to the load by drawing an isolated (not connected to anything) straight wire. Label one end Vin and one end Vout. You've now connected your voltage source through an output impedance Ros to a load resistance RLoad. Check that the voltage Vin (=Vout) is ½ of the source voltage.

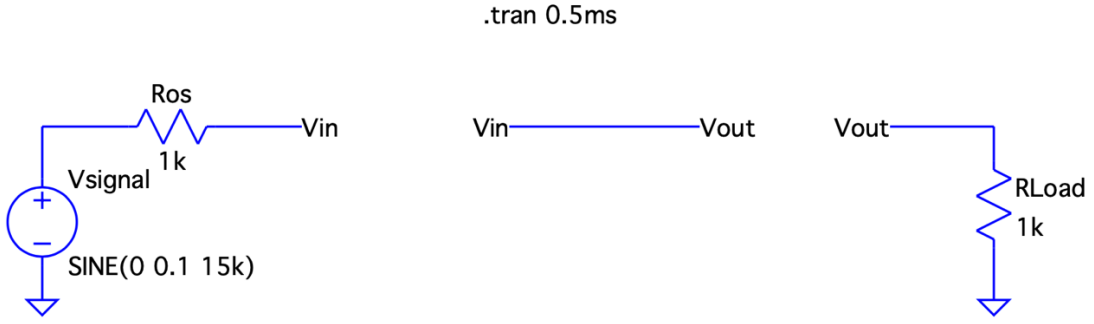

Figure 1

The connection works because the two different wire ends have the same label, so it's as if a wire was connected between them.

Step 2: The Common Emitter Amplifier

Once you have verified that the circuit in Fig. 1 is working as expected, now construct the common emitter amplifier shown in Fig. 2, along with a signal source and a load (you can just edit the step 1 circuit, removing the single wire and replace it with the transistor circuit). The transistor component is just called npn in LTSpice. Note that the 15V supply is sitting off to the side using a label VCC to connect it to the common emitter circuit. Be careful to label the Vin, Vout and Vcc nodes or your hidden wire connections will be missing.

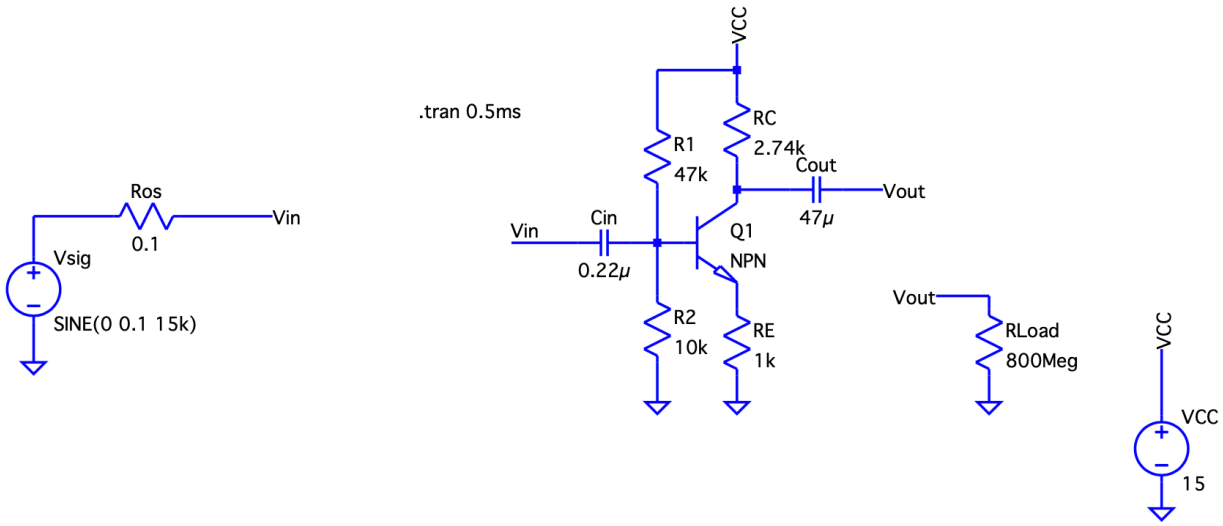

Figure 2 – Signal Generator, Common Emitter Amplifier and Load

(a) Turn off your signal by setting the amplitude to 0V and make the load so large as to effectively be an open circuit (e.g. 100MEG). Now determine the quiescent voltages at the base (V_B), collector(V_C), and emitter(V_E) of the transistor. Determine h_{FE} (β) for the transistor by measuring the current into the base I_B and the current into the collector I_C ($I_C = h_{FE}I_B$). Note that LTSpice uses a different drop than our canonical 0.6V between V_B and V_E. Verify that the quiescent voltages are roughly what you predicted in the prelab for Lab 7.

(b) Now we'll test the circuit with an AC signal. Set Ros to 0.1 Ohm (making this an ideal signal source) and the voltage signal to 100 mV. Make a plot of Vin and Vout on the same graph and include it in your lab notebook. Determine the gain and compare to the prediction for the common emitter circuit.

(c) As you learned in Lab 7, if the output signal is too large, the output will be clipped. Leaving the load "infinite" and the source impedance Ros at 0.1 Ohm, increase the signal amplitude until you observe clipping of the output. Record the value of the input amplitude where clipping occurs. Using an input somewhat *larger* than this clipping value (in which both min and max are clipped), make a plot of V_C and V_E on the same graph and include it in your lab notebook. Explain why the output is clipped at the maximum V_C and why it is clipped at the minimum V_C (they are clipped for different reasons!).

(d) In the prelab for Lab 7, you calculated the input and output impedances for the common emitter amplifier. We will test them here by changing the signal output impedance and the load. First set the signal output impedance Ros to be the same as the input impedance you calculated for the common emitter amplifier ((rin||R1||R2) where rin = $R_E h_{FE}$). If you are close to correct, the voltage divider should make your Vin about half of the amplitude of the voltage supply. Change Ros until Vin is close to 50% of the signal amplitude of 100mV. You've now determined the input impedance! Record in your lab notebook. Which part of this particular circuit plays the major role in determining the input impedance: the intrinsic impedance of the transistor rin or the voltage divider providing the base bias R1||R2?

(e) Now reset Ros to 0.1 Ohm. Find the output impedance of the common emitter by changing RLoad until Vout is 50% of the value of Vout when RLoad is "infinite." After recording in your lab notebook, compare to the prediction from the prelab of Lab 7, rout = RC.

Step 3: Dual Stage amplifier (common emitter into emitter follower)

While the common emitter amplifier can have a good gain and a large input impedance, the problem with it is that it has a large output impedance, so that a typical load of a few 100 Ohm (or less for a speaker) gets almost no output voltage across the load (remember, no sound out of the speaker!). The solution is to feed the output into a follower, which reproduces the signal with gain of 1, but has a much lower output impedance.

(a) Save your common-emitter circuit into a file with a separate name so that you can edit it to become the dual stage amplifier without losing your common emitter circuit file. Now add the emitter follower stage as shown in Fig. 3. Note that you do not need a coupling capacitor in between the output of the common emitter and the input to the emitter follower, but you do need it on the output of the follower.

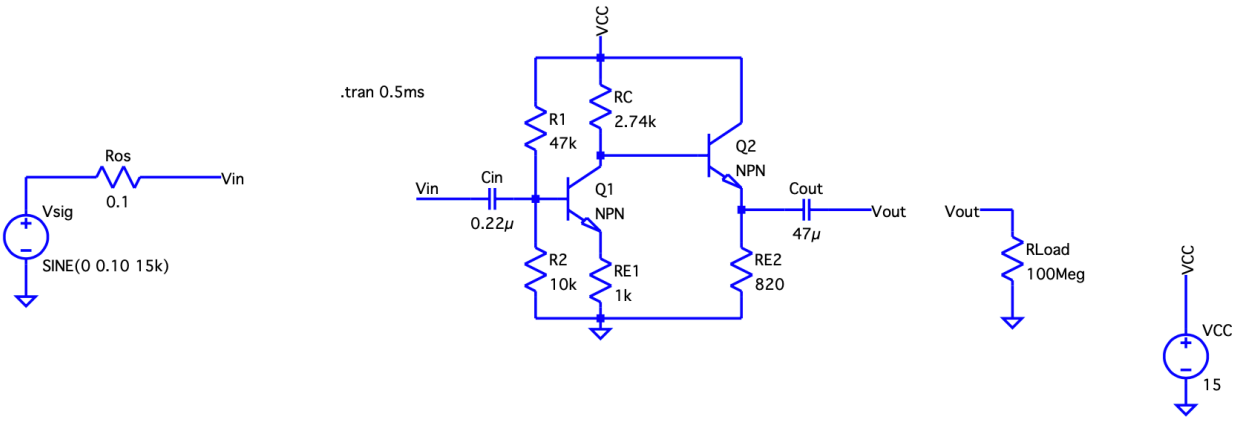

Figure 3

(b) Test your circuit using the ideal input of 100 mV with Ros = 0.1 Ohm and the "infinite" load (e.g.100MEG). Verify that you get the same gain as the common emitter circuit of the previous step. Using the same procedures as in step 2 (d) and (e), determine the input and output impedances of the dual stage amplifier (one at a time!). First keep RLoad large and change Ros until Vin is half of Vsig. Then set Ros back to 0.1 and decrease RLoad until you decrease Vout to half of the output with 100MEG (not half Vsig). Do these agree with the predictions from the prelab 7? The dual stage is more complicated, but one can still analyze the circuit by thinking about the stages in sequence.

(c) To see the effect of the dual stage, measure Vout for the single stage common emitter (from Step 2) with a load of 100 Ohms and then measure Vout with the dual stage amplifier, also with a load of 100 Ohms. By what factor did the dual stage amplifier increase Vout for this load?

Step 4: The Darlington Pair

Another useful and common BJT amplifier is the so-called Darlington Pair. In this case, the emitter of one transistor is directly connected to the base of a second emitter. Since $I_C = h_{FE} I_B$, and $I_E \approx I_C$, the collector current in the second transistor is approximately h_{FE}^2 times the base current in the first transistor. This large current gain means that the input signal can be much smaller. It also has the advantage of having a large input impedance and small output impedance. A Darlington pair emitter-follower is shown in Fig. 4. Darlington pairs are so widely used that you can buy chips with the Darlington pair internally connected in the chip, with three leads: for the common VCs, the input base and the output emitter.

(a) In a separate .asc file, create the Darlington pair emitter-follower shown in Fig. 4, along with the standard signal source and load. Initially keep Ros at 0.1 and RLoad at 100MEG.

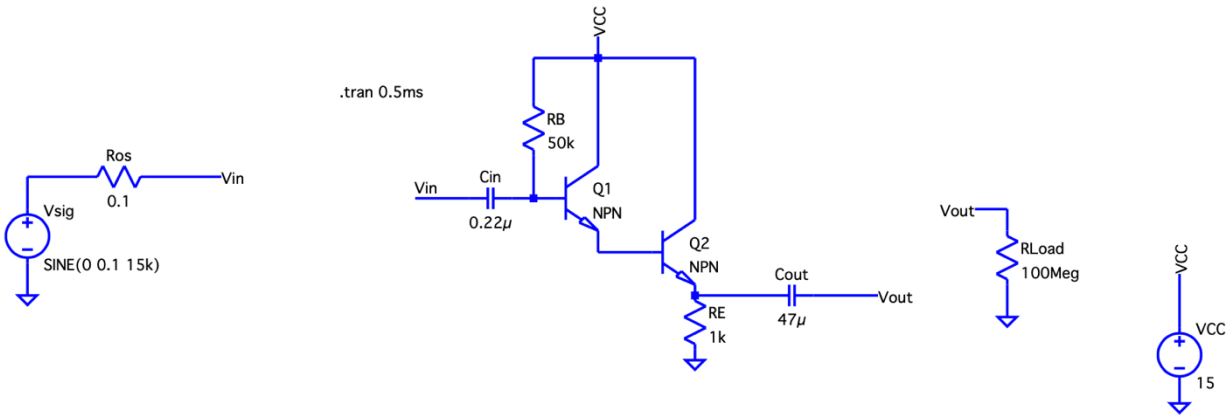

Figure 4

(b) Set the signal amplitude to zero and look at the quiescent voltages at collector, emitter and base for each transistor. Note that a "drawback" of this configuration is a "double" drop between the base of Q1 and the emitter of Q2. Does the collector current in the second transistor have h_{FE}^2 times the base current into the first transistor? Notice that the bias on the first transistor base is not the same as a voltage divider, as used in the common emitter bias. In fact the output doesn't depend on RB much unless it is too small, since the base current into first transistor is small. We'll test this in a moment.

(c) Now set the signal amplitude to be 100 mV. Plot Vin and Vout on the same plot and find the gain of this circuit. Change RB by a factor of 2 larger and a factor of 2 smaller. What change, if any, do you see in the gain?

(d) Again, by adjusting Ros and RLoad separately (as in Step 3(d)), determine the input and output impedances of the Darlington pair (don't forget to return RB to its original value). Compare to the approximate formulas that Rin = RB||rin and rin = $(h_{FE})^2$RE and Rout = (RB||Ros)/$(h_{FE})^2$. Note that LTSpice may hangup or crash if you try to determine the output impedance with a very small Ros. So for that test, make Ros something large, like 50k Ohms.

Step 5: A PNP transistor circuit

While not common, you may at some point need to use a PNP transistor, so let's build our common emitter amplifier using a pnp transistor, so you can see the difference. The key is the arrow on the emitter, which shows the direction of current flow into the emitter and out of the base and collector (just the opposite of the NPN). Now the base and collector have to be at voltages lower than the emitter. Figure 5 shows our common emitter amplifier with a PNP transistor with the collector pulled down to a negative supply instead of a pulled up to a positive supply; note that nothing else has changed! Sometimes the choice of NPN over PNP is totally driven by power supply polarity, though this is more usually an issue with power applications rather than amplifier applications. Note we also could have connected RE to +15 V and connected RC to ground.

(a) Make a copy of your NPN common emitter and edit it to have a PNP transistor and change the VCC from +15 to -15V, as shown in Fig. 5. Setting the signal to 0 amplitude, determine the quiescent voltages at the base, emitter and collector terminals. Determine h_{FE} for the PNP transistor by comparing the base and collector currents (easiest with quiescent values).

(b) Determine the gain with a 100 mV signal, Ros = 0.1 and “infinite” (100MEG) load. Next determine the signal amplitude where clipping occurs; is it the same as with the NPN transistor?

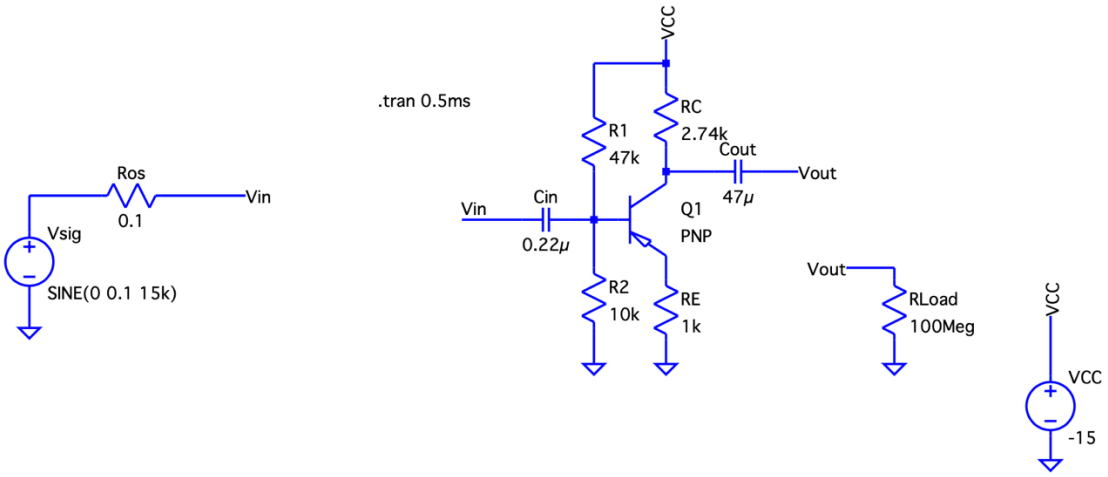

Figure 5

We have only scratched the surface of applications using BJT transistors, but you should now have a better idea of how they work, and how to choose biases. The major complication we have only touched on is the Eber-Moll model where the current dependent emitter resistance is significant. Note that it is in LTSpice! You can see it’s effect if either RE or RLoad get very small (order of a 10 ohms).

Appendix: Number convention of LTSpice (Modified from Wikipedia)

SPICE Suffix[26]	Metric Name	English Name	Power of 10	Numeric Value	Notes and Common Mistakes
u or µ	micro	Millionth	10^{-6}	0.000001	Older SPICE software does not support theµ(Mu) character
T	tera	Trillion	10^{12}	1000000000000	
p	pico	Trillionth	10^{-12}	0.000000000001	
n	nano	Billionth	10^{-9}	0.000000001	
mil	thou		25.4×10^{-6}	0.0000254	milis a thousandth of an inch(0.001") which is 25.4 µm[26]
MEG	mega	Million	10^{6}	1000000	Wrong use ofm/meg/mil are common mistakes in all SPICE programs
m	milli	Thousandth	10^{-3}	0.001	"1m" & "1M" doesn't mean "1megaohm, instead "1MEG" is correct[1]
K	kilo	Thousand	10^{3}	1000	
G	giga	Billion	10^{9}	1000000000	

- The suffix (left column) is case insensitive.[1] For example, 1MEG / 1meg / 1Meg represents 1000000; 1k / 1K represents 1000.
- Any appended text after the suffix (left column) is ignored.[1] For example, 2MegHz / 2MegaOhm represents 2000000; 3mV / 3mOhm represents 0.003.
- In LTSpice, any suffix (left column) can replace the decimal point of a real number, a common format for printed schematics.[1] For example, 4K7 represents 4700, 1u8 represents 0.0000018.

[1] LTSpice - General Conventions". *Ltwiki*. Archived from the original on December 5, 2018.